Our Docket No.: 042390.P7045D
Express Mail No.: EL802873113US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
RAMALINGAM, ET AL.	Examiner:
Application No.:	Art Group:
Filed:	
For: Controlled Collapse Chip Connection (C4) Integrated Circuit Package Which has Two Dissimilar Underfill Materials	
DIVISIONAL of Application:	
Application No.: 09/261,849	
Filed: March 3, 1999	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231-9998

Sir:

The subject Application, a divisional of the above-identified parent Application, is being filed concurrently. Applicant respectfully requests amending the subject Application as follows:

IN THE SPECIFICATION

On page 1, line 10 before "**BACKGROUND OF THE INVENTION**", please insert the following:

A-1

--CROSS-REFERENCES TO RELATED APPLICATIONS

This Preliminary Amendment is filed concurrently with a Divisional Application under 37 C.F.R. §1.53(b). Applicants respectfully request the Examiner to examine these claims as now amended.

IN THE CLAIMS

Following is a complete set of claims as amended with this Response. This complete set of claims excludes claims 1-6, cancelled without prejudice, and includes amended claims 8-16 and new claims 17-25.

7. A process for underfilling an integrated circuit that is mounted to a substrate, comprising:

dispensing a first underfill material which becomes attached to the integrated circuit and the substrate; and,

dispensing a second underfill material which become attached to the integrated circuit and the substrate.

8. (Amended) The process as recited in claim 11, wherein the first underfill material flows between the integrated circuit and the substrate.

A2

9. (Amended) The process as recited in claim 8, wherein the substrate moves within an oven while the first underfill material flows between the integrated circuit and the substrate.

10. (Amended) The process as recited in claim 11, wherein the second underfill material is dispensed in a pattern which surrounds the first underfill material.

11. (Amended) A process for underfilling an integrated circuit that is mounted to a substrate comprising:

heating the substrate before a first underfill material is dispensed;

dispensing the first underfill material which becomes attached to the integrated circuit and the substrate; and,

dispensing a second underfill material which become attached to the integrated circuit and the substrate.

12. (Amended) The process as recited in claim 11, further comprising heating the first underfill material to a partial gel state.

13. (Amended) The process as recited in claim 12, wherein the substrate is heated to a temperature that is greater than a temperature for heating said first underfill material to said partially gel state.

14. (Amended) The process as recited in claim 11, further comprising mounting the integrated circuit to the substrate with a solder bump before the first underfill material is dispensed.

15. (Amended) A process for mounting and underfilling an integrated circuit to a substrate, comprising:

baking the substrate;

mounting an integrated circuit to the substrate;

dispensing a first underfill material onto the substrate, the first underfill material flows between the integrated circuit and the substrate while the substrate moves through an oven; and,

dispensing a second underfill material around the first underfill material.

16. (Amended) The process as recited in claim 15, further comprising mounting the integrated circuit to the substrate with a solder bump before the first underfill material is dispensed.

17. (New) The process as recited in claim 15, wherein the baking of said substrate occurs before said first underfill material is dispensed.

18. (New) The process as recited in claim 15, wherein prior to dispensing the second underfill material, the method further comprises heating the first underfill material to a partial gel state.

19. (New) The process as recited in claim 18, wherein the substrate is baked at a temperature that is greater than a temperature for heating said first underfill material to said partially gel state.

20. (New) The process as recited in claim 19, wherein said temperature for heating said first underfill material to said partially gel state is greater than a temperature at which said second underfill material is dispensed.

21. (New) The process as recited in claim 13, wherein said temperature for heating said first underfill material to said partially gel state is greater than a temperature at which said second underfill material is dispensed.

a3

22. (New) A process for mounting and underfilling an integrated circuit to a substrate, comprising:

heating the substrate to a first temperature;

mounting an integrated circuit to the substrate;

dispensing a first underfill material onto the substrate and heating the first underfill material to a second temperature in which the first underfill material is in a partial gel state and flows between the integrated circuit and the substrate while the substrate moves through an oven; and,

dispensing a second underfill material around the first underfill material.

23. (New) The process as recited in claim 22, further comprising mounting the integrated circuit to the substrate with a solder bump before the first underfill material is dispensed.

24. (New) The process as recited in claim 22, wherein the first temperature is greater than the second temperature.

25. (New) The process as recited in claim 24, wherein the second temperature is greater than a temperature at which the second underfill material is dispensed.

REMARKS

Applicants file the divisional application while a related U.S. patent application (App. No. 09/261,849) is co-pending.